CLAIMS

1. A calibrated filter comprising:

an RC filter having tunable capacitors having a capacitive value responsive to a control code;

a fully differential calibration circuit comprising:

a differential operational amplifier;

a differential voltage source;

a first resistor selectively coupled between a first terminal of the differential voltage source and a first integrating capacitor coupled across a first input and a first output of the differential operational amplifier;

a second resistor selectively coupled between a second terminal of the differential voltage source and a second integrating capacitor coupled across a second input and a second output of the differential operational amplifier;

a logic circuit for:

charging the first and second capacitors through the first and second resistors over a first predetermined number of clock periods;

discharging the integrating capacitors by a predetermined voltage over a second predetermined number of clock periods; and

counting the number of clock periods to needed to discharge the integrating capacitors to a predetermined voltage level to generate the control code for tuning the tunable capacitors.

2. The calibrated filter of claim 1 wherein the fully differential calibration circuit includes a differential operational amplifier coupled to a differential comparator circuit.

3. The calibrated filter of claim 1 wherein the calibration circuit has a symmetrical correction range.

4. The calibrated filter of claim 3 wherein the correction code is asymmetrical for the nominal capacitive value.

5. The calibrated filter of claim 4 wherein the first and second resistors have a nominal value *R* and the first and second capacitors have a nominal value *C*, and where $RC=4/3T_C$, where T_C equals a clock period.

6. A method of calibrating a filter, comprising the steps of:

providing an RC filter having tunable capacitors having a capacitive value responsive to a control code;

providing a fully differential calibration circuit comprising a differential operational amplifier, a differential voltage source, a first resistor selectively coupled between a first terminal of the differential voltage source and a first integrating capacitor coupled across a first input and a first output of the differential operational amplifier, and a second resistor selectively coupled between a second terminal of the differential voltage source and a second integrating capacitor coupled across a second input and a second output of the differential operational amplifier;

charging the first and second capacitors through the first and second resistors over a first predetermined number of clock periods;

discharging the integrating capacitors by a predetermined voltage over a second predetermined number of clock periods; and

counting the number of clock periods to needed to discharge the integrating capacitors to a predetermined voltage level to generate the control code for tuning the tunable capacitors.

7. The method of claim 6 and further comprising the step of driving a comparator circuit with the differential operational amplifier.

8. The method of claim 6 and further comprising the step of biasing the correction code to provide a symmetrical correction range.

9. The method of claim 4 wherein the first and second resistors have a nominal value *R* and the first and second capacitors have a nominal value *C*, and further comprising the step of setting $RC=4/3T_C$, where T_C equals a clock period.